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Docket No.: GR 99 P 1058

Date: January 18, 2000


XIOMARA D. JUNCO

Hon. Commissioner of Patents and Trademarks
Washington, D.C. 20231

Sir:

Enclosed herewith are the necessary papers for filing the following application for Letters Patent:

Applicant : Wilfried Dähn

Title : Integrated Semiconductor Circuit and Method for Functional Testing of Pad Cells

2 sheets of formal drawings in triplicate.

A check in the amount of \$690.00 covering the filing fee.


Claim for Priority. Certified copy of the corresponding foreign patent application No. 199 01 460.4, filed January 15, 1999.

Information Disclosure Statement and 3 References.

This application is being filed without a signed oath or declaration under the provisions of 37 CFR 1.53(d). Applicant awaits notification of the date by which the oath or declaration and the surcharge are due, pursuant to this rule.

The Patent and Trademark Office is hereby given authority to charge Deposit Account No. 12-1099 of Lerner and Greenberg, P.A. for any fees due or deficiencies of payments made for any purpose during the pendency of the above-identified application.

Respectfully submitted,


For Applicant
LAG:bb

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INTEGRATED SEMICONDUCTOR CIRCUIT
AND METHOD FOR FUNCTIONAL TESTING OF PAD CELLS

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Background of the Invention:

Field of the Invention:

The invention relates to an integrated semiconductor circuit having pad cells, and to a method for functional testing of
10 the pad cells.

Integrated semiconductor circuits have pad cells which include a connecting pad with a flat connecting area for external supply lines, and an upstream output driver. The external
15 supply lines are used to interchange data or signals between different circuits or assemblies, and the output drivers which are integrated in the pad cells are used to output digital signals to the external supply lines. In order to provide reliable operation of the integrated circuit and of assemblies
20 connected to the circuit, the serviceability of the output drivers must satisfy requirements which are specified in detail, particularly with regard to the transmission response for signals.

25 It is necessary to test the serviceability of the circuit, and thus of the individual pad cells, particularly in conjunction

with the production of an integrated circuit. In order to do that, it is normal to take measurements to characterize the transmission response of the pad cells. The measurements provide information about the dynamic response of a pad cell to various types of signal excitation. Such signal excitations are, for example, step-function signal changes from a low signal level to a high signal level, or vice versa. The output signal response of the tested pad cell to step-function signal excitations is characterized by dynamic delays of signal transitions. During functional testing, the signal time response of the output of the pad cell is measured and is then investigated to determine whether or not that dynamic response of a pad cell is within specified tolerances. The measurements which are required for that purpose at precisely defined times must be carried out in that case at highly accurate times. The accuracy is located in the region of less than 100 ps (picoseconds) with the present state of development.

Those measurement accuracy requirements involve a high level of equipment complexity, and thus very complex and costly test facilities. However, the above-described stringent requirements for time accuracy of the test facilities are generally not required for other functional tests of integrated circuits.

Summary of the Invention:

It is accordingly an object of the invention to provide an integrated semiconductor circuit and a method for functional testing of pad cells, which overcome the hereinafore-mentioned disadvantages of the heretofore-known devices and methods of this general type and with which it is possible to carry out a functional test of a transmission response of the pad cells with a relatively low level of equipment measurement complexity.

With the foregoing and other objects in view there is provided, in accordance with the invention, an integrated semiconductor circuit, comprising at least one pad cell to be monitored in a first operating mode of the circuit by a functional test, the at least one pad cell each having a connecting pad, an upstream output driver and a connection for an input signal; and a signal transmitter for producing periodic signal sequences, the signal transmitter having a connection for a periodic output signal connected to the connection for an input signal of the at least pad cell to be tested, in order to test a transmission response of the at least one pad cell in the first operating mode. Application of a periodic signal to the pad cell allows a measurement to be carried out externally, in the frequency domain, at the output of the pad cell.

With the objects of the invention in view there is also provided a method for testing a transmission response of pad cells each including a connecting pad and an upstream output driver, in an integrated semiconductor circuit, which

5 comprises connecting an output of a pad cell to be tested to a measurement input of a measurement configuration suitable for spectrum analysis; and measuring a transmission response of the pad cell in a frequency domain using the measurement configuration.

10 In this way, the dynamic response of the pad cell can be characterized. The requirements for the resolution of the measurement in the frequency domain and thus the equipment complexity of the measurement device can be kept low since,

15 according to the invention, the detection of harmonics up to the fifth harmonic is adequate for sufficiently accurate analysis and the frequency separation between these harmonics is relatively large.

20 In accordance with another feature of the invention, the signal transmitter can be reprogrammed in order to produce different periodic signal sequences. It is thus possible to match the measurement to the characteristic of pad cells with different switching speeds. For example, that is done through

25 the use of a signal sequence with a short period duration for relatively fast-switching output drivers, and a signal

sequence with a longer period duration for relatively slow-switching output drivers.

In accordance with a further feature of the invention, if a plurality of pad cells have to be tested, the inputs of the pad cells to be tested can be connected in parallel to one or more connections for the output signal from the signal transmitter, or can be connected in series, for example through one shift register cell in each case, to a connection for the output signal from the signal transmitter. All of the pad cells to be tested thus receive the same input signal, that is delayed by one clock period in each case.

In accordance with a concomitant feature of the invention, in order to make it possible to switch over between the normal mode and the test mode as easily as possible, it is advantageous to connect a multiplexer circuit in each case between the input of the pad cell and the output from the signal transmitter. The multiplexer circuit is controlled, for example, by an operating mode controller.

Other features which are considered as characteristic for the invention are set forth in the appended claims.

Although the invention is illustrated and described herein as embodied in an integrated semiconductor circuit and a method

for functional testing of pad cells, it is nevertheless not intended to be limited to the details shown, since various modifications and structural changes may be made therein without departing from the spirit of the invention and within
 5 the scope and range of equivalents of the claims.

The construction and method of operation of the invention, however, together with additional objects and advantages thereof will be best understood from the following description
 10 of specific embodiments when read in connection with the accompanying drawings.

Brief Description of the Drawings:

Fig. 1 includes an upper part which is a schematic and block
 15 circuit diagram of a configuration for measuring a dynamic response of a pad cell, and a lower part which is a graph of an example of a profile of a step-function response of an output of the pad cell;

20 Fig. 2 is a schematic and block circuit diagram of an output driver of a pad cell, with model parameters; and

Figs. 3 and 4 are block circuit diagrams of exemplary embodiments of an integrated circuit according to the
 25 invention, having a plurality of pad cells to be tested.

Description of the Preferred Embodiments:

Referring now to the figures of the drawings in detail and first, particularly, to Fig. 1 thereof, it is seen that an upper part of the figure shows a configuration for functional

5 testing of a pad cell PC of an integrated circuit. This configuration is intended to be used to characterize a transmission response of an output driver of the pad cell PC in a test mode. To this end, a digital signal U_E which is equivalent to a step-function from a low signal level to a

10 high signal level is applied to an input E of the pad cell PC (connection for the input signal of the output driver). In addition, a signal profile of a signal U_{DQ} of an output DQ of the pad cell PC is measured (connection for the supply line to be connected to the connecting pad). This signal profile

15 characterizes a dynamic response of the pad cell PC, which can be simulated, with model parameters, by using an equivalent circuit. An example of a circuit diagram of an output driver of a pad cell PC with model parameters R_{D1} , R_{D2} , L, C is shown in Fig. 2.

20 A lower part of Fig. 1 shows a simplified profile of the so-called step-function response of the signal U_{DQ} resulting from the step-function of the signal U_E . A voltage level of the signal U_{DQ} in this case does not rise suddenly from a switch-on

25 time t_1 to a value U_H in the steady state, but correspondingly more slowly in a dynamic response corresponding to values of

the model parameters R_{D1} , R_{D2} , L , C , characterized by a time constant t . As is generally known, its magnitude depends on the values of the model parameters R_{D1} , R_{D2} , L , C .

5 A criterion for serviceability of a pad cell PC in Fig. 1 is that the voltage level of the signal U_{DQ} between a minimum time t_{min} and a maximum time t_{max} from the switch-on time t_1 has a value which is in a tolerance range between a minimum value U_{min} and a maximum value U_{max} . A profile 1 of the signal U_{DQ}

10 shows an example of a step-function response of a serviceable pad cell PC. A profile 2 of the signal U_{DQ} shows an example of the step-function response of a faulty pad cell PC. The time period between t_{min} and t_{max} with the present state of development is a few hundred picoseconds, which means that the

15 measurement accuracy of the measurement apparatus is subject to comparatively stringent requirements. These requirements have the consequences that have already been mentioned initially, particularly with regard to high procurement costs.

20 Fig. 3 shows a circuit configuration having a single transmitter SG in order to produce periodic signal sequences. If the inputs E of the pad cells PC are stimulated with a periodic signal sequence, a periodic profile of the output signals U_{DQ} can likewise be observed at their outputs DQ. That

25 profile, depending on the characteristic of the input signal, is composed of a DC element, a fundamental frequency and

harmonics. This profile can be measured by using a measurement method with a measurement configuration SAZ having a measurement input which is connected externally to the output DQ. The measurement configuration SAZ is suitable for carrying out a spectrum analysis, for example with a so-called spectrum analyzer, and can be characterized by an analysis of the recorded frequency spectrum.

Depending on the accuracy which is required for testing the transmission response, a more or less detailed equivalent circuit of the pad cell PC to be tested is produced with more or less different types of model parameters, depending on the level of detail. In the example shown in Fig. 2, the pad cell PC was characterized by model parameters R_{D1} , R_{D2} , L and C .

Resistances R_{D1} and R_{D2} in this case model switched-on resistances of switching transistors T1 and T2, an inductance L models supply line inductances, and a capacitance C models line capacitances. In an evaluation carried out after the measurement, the values of the previously defined model parameters for the pad cell PC are determined successively in a known manner (for example through the use of a Fourier analysis) from the frequency spectrum, which includes the amplitude response and/or the phase response. Those values are used to calculate the step-function response of the pad cell PC, which provides information as to whether or not the criterion for serviceability is satisfied. In this context,

it is also possible to ascertain the step-function response by using the known analysis method directly from the frequency spectrum, without having to produce an equivalent circuit with model parameters beforehand.

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The number of harmonics to be determined in the frequency spectrum is governed essentially by the number of model parameters being defined. The greater the number of model parameters that must be defined, the greater the number of harmonics to be detected. These are detected in rising sequence starting with the fundamental, and the amplitude response and/or phase response are/is recorded. It is known from experience that determination up to the fifth harmonic is sufficient for adequate accuracy. Since these are the only harmonics which are detected, and their frequency separation is relatively large in comparison with the harmonics above the fifth harmonic, the complexity of the measurement apparatus with regard to frequency selectivity remains relatively low. Consequently, it is considerably less than for a described measurement in the time domain. The step-function response is calculated through the use of the time constant t , which is calculated by using the values of the model parameters.

In the case of relatively slow-switching pad cells PC, the line inductance L as well as a load capacitance C_l and the line capacitance C can be ignored in comparison with the switched-

on resistances R_{D1} , R_{D2} of the transistors T1 and T2. The measurement in the frequency domain can therefore be replaced by a simple direct-current measurement at the output DQ. Values of supply voltages V_{CC} and V_{SS} and currents I_1 and I_2 allow the respective resistances R_{D1} and R_{D2} to be calculated and thus, as mentioned above, the step-function response of the signal U_{DQ} . However, in order to carry out this measurement, it is necessary to increase the period duration of the stimulating input signal U_E , so that a virtually steady state exists at the output DQ for each measurement of the currents I_1 and I_2 . The period duration of the signal U_E can be changed, for example, by reprogramming the signal transmitter SG through the use of an external control signal BS from an operating mode controller.

Fig. 3 shows an exemplary embodiment of the circuit according to the invention, from which it can be seen that the inputs E of a plurality of pad cells PC to be tested are connected in parallel to a connection A for the periodic output signal from the signal transmitter SG. A variant is also conceivable in which, if there are a plurality of outputs A from the signal transmitter SG, each individual output is connected in parallel to a respective one of the inputs E of the pad cell PC.

A multiplexer circuit MUX is provided in order to switch over between a test mode for functional testing of the pad cells PC as a first operating mode of the integrated circuit, and a normal mode as a second operating mode of the integrated circuit. A respective multiplexer circuit MUX is connected between the output A of the signal transmitter SG and each connection E for the input signal of the pad cells PC and is also controlled, for example, by the signal BS from an operating mode controller. In addition to one input to which the output signal from the signal transmitter SG is applied, another input of the multiplexer circuit MUX is provided in each case for a signal 0 to n, which can be output in the normal mode to another functional unit FE in the integrated circuit.

Fig. 4 shows a further exemplary embodiment of the circuit according to the invention. In this case, the connections E for the input signals of a plurality of pad cells PC to be tested are each connected in series through a respective clock-controlled shift register cell FF0 to FF_n to a connection A for the output signal from the signal transmitter SG. Consequently, the periodic output signal from the signal transmitter SG is applied to each pad cell PC, in each case delayed by one clock period of the shift register cells FF0 to FF_n. This exemplary embodiment is advantageous for circuits in which the pad cells PC are already connected to one another

through shift register cells FF0 to FF_n for other purposes
(for example for printed circuit boards with "boundary scan").

The shift register cells FF0 to FF_n and the signal transmitter
5 SG can be provided, for example, through the use of clock-
controlled bistable multivibrators. The signal transmitter SG
may, for example, be a T-flip-flop with a hard-wired input,
and the shift register cells FF0 to FF_n may be provided, for
example, by D-flip-flops. The signal transmitter SG and the
10 shift register cells FF0 to FF_n are controlled by the same
clock for this purpose. The T-flip-flops, as described above,
are advantageously constructed in such a way that the
respective periodic output signals can be varied by
reprogramming.

I claim:

1. An integrated semiconductor circuit, comprising:

at least one pad cell to be monitored in one operating mode by a functional test, said at least one pad cell each having a connecting pad, an upstream output driver and a connection for an input signal; and

a signal transmitter for producing periodic signal sequences, said signal transmitter having a connection for a periodic output signal connected to said connection for an input signal of said at least pad cell to be tested, in order to test a transmission response of said at least one pad cell in said one operating mode.

2. The integrated semiconductor circuit according to claim 1, wherein said signal transmitter is reprogrammable to produce different periodic signal sequences.

3. The integrated semiconductor circuit according to claim 1, wherein said connection of said signal transmitter for an output signal is at least one connection, said at least one pad cell is a plurality of pad cells to be tested, and said connections for an input signal of said plurality of pad cells

are connected in parallel to said at least one connection of said signal transmitter for an output signal.

4. The integrated semiconductor circuit according to claim 1, wherein said at least one pad cell to be tested is a plurality of pad cells, and shift register cells are each connected in series between said connection for an input signal of a respective one of said pad cells and said connection of said signal transmitter for an output signal.

5. The integrated semiconductor circuit according to claim 1, wherein said at least one pad cell to be tested is a plurality of pad cells, and multiplexer circuits are each connected between said connection for an input signal of a respective one of said pad cells and said connection of said signal transmitter for an output signal, to switch over between said one operating mode and another operating mode.

6. The integrated semiconductor circuit according to claim 5, including:

another functional unit having a connection for a signal;

each of said multiplexer circuits having an output connected to said connection for an input signal of a respective one of said pad cells to be tested;

each of said multiplexer circuits having one input connected to said connection of said signal transmitter for an output signal;

each of said multiplexer circuits having another input to be connected to said connection for a signal of said other functional unit;

the output signal from said signal transmitter being present at said output of said multiplexer circuits in said one operating mode; and

the signal from said other functional unit being present at said output of said multiplexer circuits in said other operating mode.

7. The integrated semiconductor circuit according to claim 1, wherein said signal transmitter contains a clock-controlled bistable multivibrator of the T-flip-flop type.

8. A method for testing a transmission response of pad cells in an integrated semiconductor circuit according to claim 1, which comprises:

connecting an output of a pad cell to be tested to a measurement input of a measurement configuration suitable for spectrum analysis; and

measuring a transmission response of the pad cell in a frequency domain using the measurement configuration.

9. The method according to claim 8, which comprises measuring at least one of an amplitude response and a phase response of a recorded frequency spectrum.

10. A method for testing a transmission response of pad cells in an integrated semiconductor circuit according to claim 1, which comprises:

connecting an output of a pad cell to be tested to a measurement input of a measurement configuration suitable for spectrum analysis; and

measuring a transmission response of the pad cell by direct-current measurement at an output of the pad cell.

Abstract of the Disclosure:

An integrated semiconductor circuit includes pad cells each having a connecting pad and an output driver. A transmission response of the pad cells is to be tested in a test mode. A signal transmitter is provided in order to produce periodic signal sequences. A periodic output signal from the signal transmitter is supplied as an input signal to an input of a pad cell to be tested. Through the use of an appropriate periodic signal at an output of the pad cell, the transmission response of the pad cell is tested in a frequency domain using a measurement method which employs a spectrum analyzer. This avoids complex measurements in the time domain, which have been carried out heretofore.

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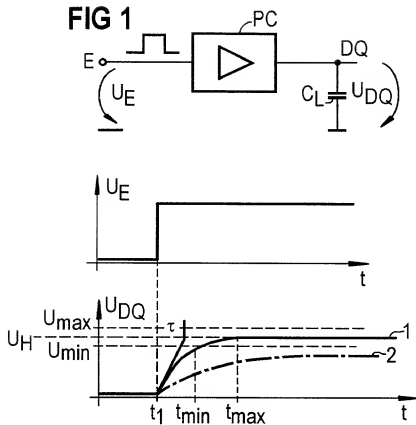
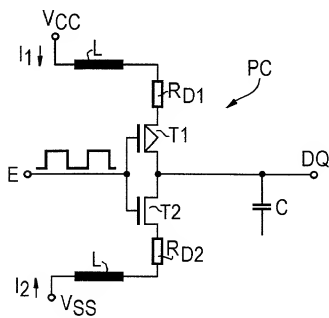
FIG 1**FIG 2**

FIG 3

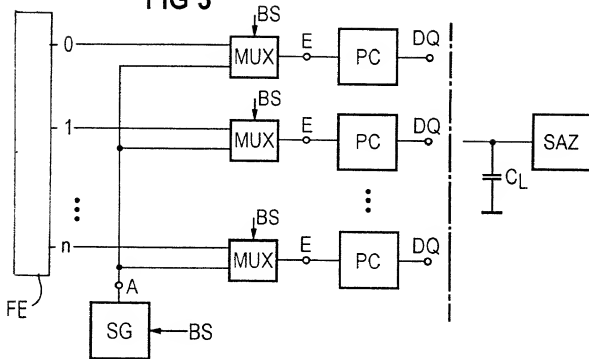
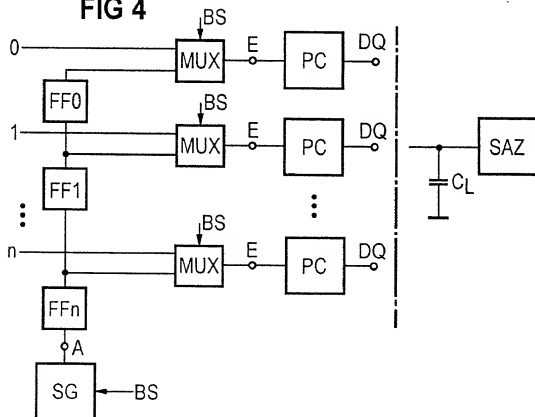


FIG 4



COMBINED DECLARATION AND POWER OF ATTORNEY
IN ORIGINAL APPLICATION

As a below named inventor, I hereby declare that: my residence, post office address and citizenship are as stated below next to my name; that I verily believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

INTEGRATED SEMICONDUCTOR CIRCUIT
AND METHOD FOR FUNCTIONAL TESTING OF PAD CELLS

described and claimed in the specification bearing that title, that I understand the content of the specification, that I do not know and do not believe the same was ever known or used in the United States of America before my or our invention thereof, or patented or described in any printed publication in any country before my or our invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve month prior to this application, that I acknowledge my duty to disclose information of which I am aware which is material to the examination of this application under 37 C.F.R. 1.56a, and that no application for patent or inventor's certificate of this invention has been filed earlier than the following in any country foreign to the United States prior to this application by me or my legal representatives or assigns:

German Application No. 199 01 460.4, filed January 15, 1999, the International Priority of which is claimed under 35 U.S.C. §119.

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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